

Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in IGBT modules



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ABSTRACT

A micro-sectioning approach for characterizing the quality or degradation state of interconnect interfaces in electronic components is described. The method is presented as a means of investigating the bonding quality of the Al wedge bonding process in IGBT modules. But in general it is applicable to any type of interface and may be used to assess the present quality of the interface. The micro-sectioning is based on mechanical polishing, chemical polishing, electro-etching, and various types of microscopy.

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1. Introduction

The lifetime and performance of an electronic device as an IGBT (Insulated Gate Bipolar Transistor) module is depending on its application area, often limited by the interconnects. Particularly the interface between the commonly used Al bond wires and the semiconductor components is a critical point due to the mismatch in the coefficients of thermal expansion. This mismatch is believed to be the dominating effect in the bond wire fatigue failure mechanism, which includes bond wire lift-off and heel cracking. In recent years the latter has become more and more rare [1–3].

The bond wire lift-off failure mechanism in IGBT modules is primarily due to fatigue crack propagation inside the wire material. This is due to the bonding quality, where the refinement of the granular structure results in a stronger interface than the material itself. Accordingly the crack is initiated in a natural area, near a void or near the interface edge, and propagates towards the wire center where the breaking strength is lower. At some point the grain size of the refinement region comes close to that of the bulk wire resulting in a change of propagation direction of the crack to a horizontal one with respect to the interface. Based on this a microscopical investigation of the wire/chip interface may yield a direct measure of the quality as well as enable a detailed reliability assessment [4,5].

Reducing the risk of interconnect related failure mechanisms is of paramount importance as these are presently the limiting factors. This has motivated a search for an alternative to the Al wire as well as to soft solders. To mention a few, the ordinary Al wire has been proposed to be substituted by ribbons, Cu, or other bonding techniques. These hold various pros and cons, where many of the disadvantages are related to production compared to the

wedge bonding applied to Al wires. Even though these methods reduce the thermo-mechanical related degradation the interconnects remain to be the weak point with respect to lifetime. Thus, an accurate knowledge of the interfaces is still of importance [6].

This article presents a micro-sectioning approach for characterizing the microscopical processes occurring at interfaces. By investigating the microscopical structure the information regarding quality as well as lifetime may be obtained. In this article, the quality of wire interfaces are investigated for a series of samples to illustrate the method. The grain distribution is derived from the results and used to evaluate the quality of the bonding by looking at the refinement area. Finally, the pros and cons of the method in general are discussed and alternative ideas are presented.

2. Theory

As briefly discussed in the introduction there is a connection between the interface strength and the microscopical structure of the Al, more precisely the grain structure of the interface. A concept which is only understood from a fracture mechanical point of view, this is presented briefly in Section 2.1.

Obtaining the grain structure of pure Al in a layered system is problematic, as the contrast in the Al is often caused by impurities. The contrast across the Al is further lowered by all the subjacent layers in the geometry. Therefore, methods like electron backscattered diffraction (EBSD) and electro-etching may be employed to promote the change in crystal structure. This is outlined in Section 2.2.

2.1. Fracture mechanics

The observations that the fractures in the wire/chip interface propagate into the wire away from the interface to a certain point are simply related to the concept of grain size refinement. This is a

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technique used to strengthen certain metals with regard to yield strength and fracture toughness. In general, these properties depend on the grain diameter d , where the relation follows the Hall–Petch equation [7]:

$$\sigma_y = \sigma_0 + k_y d^{-1/2} \quad (1)$$

where σ_y is the yield strength, k_y is the dislocation locking term which describes the yielding properties of a grain to the adjacent ones, and σ_0 is the stress required for dislocation along slip planes. Naturally, the Hall–Petch equation breaks down below certain diameters, but it has been shown to be valid on the nanometer scale [7]. From Eq. (1) it becomes clear that if the fracture toughness follows the same relation, the strength of the bond strongly depend on the refinement region.

2.2. Grain structure in aluminium

The idea of the approaches presented here is to provide images illustrating the grain structure inside the Al wire and metallization. For a large number of Al alloys this is easily done, as the impurity atoms situate themselves near the grain boundaries. However, in pure Al the only difference between grains is a change in crystal orientation. The contrast this provides is not sufficient for optical microscopy or ordinary scanning electron microscopy (SEM).

If one introduces SEM methods like EBSD the grain size and type can be obtained without influencing the structure apart from a standard polishing. The resolution of the SEM also renders it possible to obtain the structure inside the metallization, which is not the case for the method presented later using optical microscopy. However, the disadvantages is the requirement of a SEM with EBSD as well as the amount of time required to obtain the diffraction patterns.

Instead or in combination with EBSD, one may use electro-etching to provide the contrast between the grains in optical images. Here, one uses a reagent to etch the surface and the changes in crystalline structure provide different etching rates. A common approach in pure Al is to use an electrolytic procedure with Barker's anodizing reagent on the Al surface followed by an investigation using optical microscopy with polarized light. This has previously yielded clear grain structures with a strong color contrast between the different grains, see [8, p. 497]. The reason for the color contrast, however, is a bit unclear. The electrolytic method combined with Barker's reagent is referred to as an anodization, but previous investigations have shown that the increased oxide layers do not provide the optical effects for a contrast between grains. Instead the belief is that the contrast is generated by multiple reflections from a rough surface [8,9].

3. Experimental procedure

The experimental procedure presented in the following is in principal applicable on any given component. The changes necessary are minded towards the region of interest, for instance the electro-etching formulae needs to be changed depending on the material composition of the wire.

3.1. IGBT module

The component of interest is an ordinary high power IGBT module intended as a power converter in e.g. a wind turbine or in the automotive industry. In Fig. 1 the layout of the component analyzed is presented:

A single section of a module consists of a baseplate (3000 μm), a baseplate solder (100 μm), a DCB (1300 μm), $2 \times$ diode (300 μm), $2 \times$ IGBT (300 μm), and $2 \times 8 - 10$ Al wire interconnects

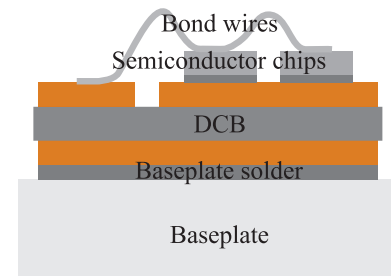


Fig. 1. Cross-sectional geometry of an ordinary IGBT module consisting of a baseplate, a direct copper bonded substrate (DCB), semiconductor chips, and Al wire interconnects [2,10].

(400 μm). Here, the thickness of the given layer is presented in the following brackets. A typical wire layout on the diode in the IGBT module is presented in Fig. 2.

The layout is similar on the IGBT chip with a larger spacing between the wires, in the type of module regarded.

3.2. Micro-sectioning

The micro-sectioning process may be divided into a macroscopic and a microscopic part. From a macroscopic stand point, the system or module of interest is cut mechanically into single components to reduce the dimensions before the microscopic handling. For an IGBT module this involves isolating the semiconductor components from each other, but also to remove unnecessary layers like a baseplate. The microscopic sectioning includes the fine mechanical polishing to the desired interface, the chemical polishing, and the electro-etching for producing grain structures in the Al.

The given chip is cast two times in order to protect the fragile components. If the geometry is to be electro-etched an electrical connection should be made to the metal prior to casting. The procedures are the following:

1. Dividing module into subelements (IGBT, diode, etc.) by mechanical cutting. This may be carried out prior to or after the initial casting into epoxy.
2. Removal of baseplate, baseplate solder, DCB, and semiconductor solder by cutting, diamond polishing, and fine-grade SiC polishing. The solders are removed to prevent the layer from affecting the electro-etching and the remaining to simplify the polishing.
3. Second cast and polishing to desired wire interface using fine-grade SiC and 3 μm diamond polishing.
4. Chemical polishing for removal of mechanical polishing lines.

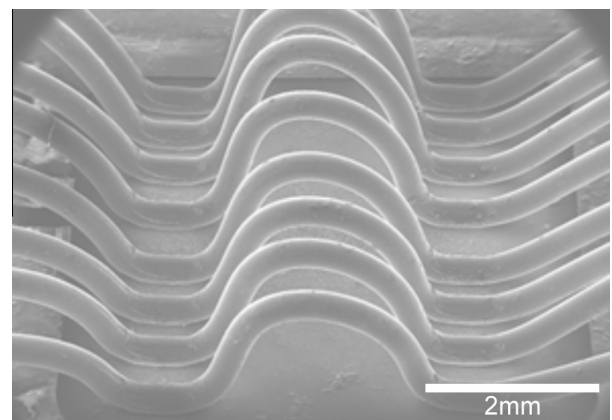


Fig. 2. SEM image of wire layout on top of the diode.



Fig. 3. IGBT chip cast into epoxy and subjected to polishing until a side view of the wire interface is reached.

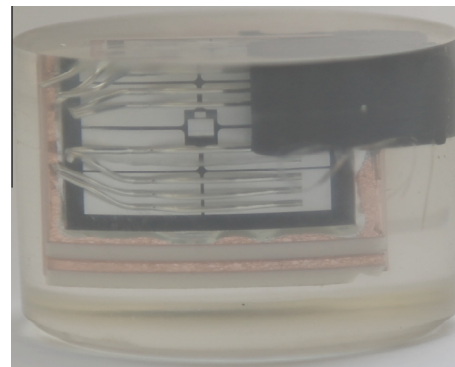


Fig. 4. Top view of the cast presented in Fig. 3.

5. Electro etching of wire/chip interface. Barker's reagent designed for promoting grain structures in pure Al. The sample is electro etched with 30 V for 2.5 min with magnetic stirring of the reagent.

An IGBT chip cast into epoxy is illustrated in Figs. 3 and 4.

One should keep in mind that the softness of the Al complicates the procedure. During the SiC polishing material from the surrounding layers as well as grains from the SiC paper may be embedded in the wire. This should be removed in the final 3 μm diamond polishing.

4. Results

The method presented in Section 3.2 is carried out for a series of samples. In general the samples are of the type presented in Section 3.1 with different types of wire. Additional parameters are varied in order to establish a proper quality investigation of the bonding process. These parameters are not subjects of the current investigation. In this paper results obtained using the micro-sectioning approach are presented together with SEM images to illustrate the method and its advantages. Afterwards, a damaged interface is presented to illustrate the reliability possibilities of the approach.

In Figs. 5 and 6 SEM images of Al wire bond interfaces are presented. In Fig. 5 the observed wire is on top of the diode whereas in Fig. 6 the interface is on the IGBT. Prior to obtaining the images the wire has been partly pried off to be able to reach the interface.

In Fig. 5 two focused ion beam (FIB) cuts are made into the surface to see the composition inside. The wire print observed is left-over material from the removal of the wire. It was possible to observe the granular structure of both the metallization and the wire in the cross-sectional image of the well produced by the cut.

A similar cross-section is shown in Fig. 6 for the cut made on the IGBT. One can see the leftovers of the wire, the metallization layer, and a part of the silicon chip. Furthermore, the grain structure is visible inside the metallization and wire but with a limited contrast. The void or partly cracked area on the right side is believed to have been created by the prying of the wire.

In Figs. 7 and 8 optical microscopy images of cross-sections of wire bond interfaces obtained through the micro-sectioning approach are presented. In both cases the bond is on top of the IGBT chip which is clear from the trench gate structure seen below the interface.

The image in Fig. 7 is an ordinary bright field (BF) microscopy image, and apart from the gate structure no mentionable objects are apparent.

In Fig. 8 the same type of image as in Fig. 7 is obtained but with electro-etching of the surface and use of polarized light. A clear granular structure is seen where the diameter of the grains ranges in size up to 20 – 40 μm . The smallest grains resolved by the microscope are about 5 μm . Furthermore, a clear change in grain struc-

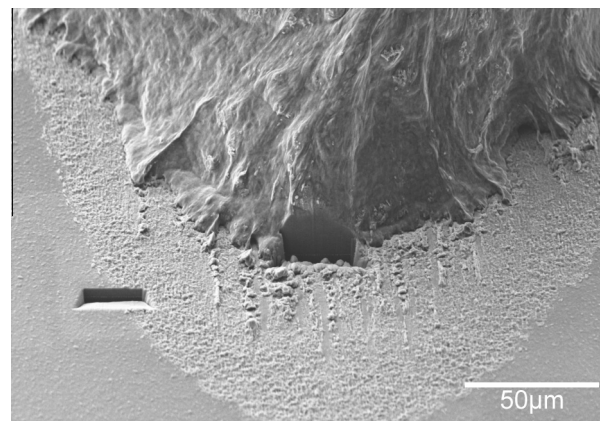


Fig. 5. SEM image of the heel of an Al wire bonding. Two FIB cuts has been carried out, one inside the wire interface and one near the edge of the interface after the wire has been pried off.

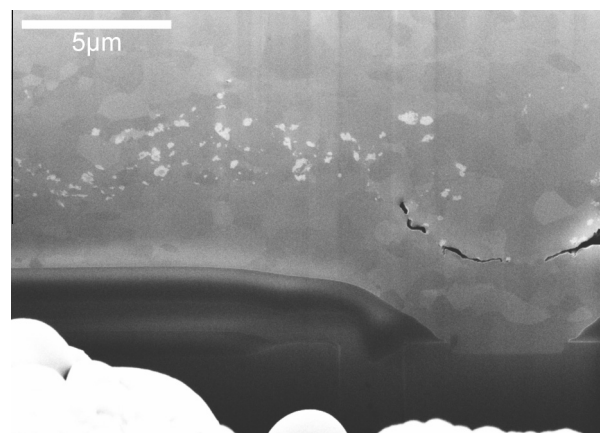


Fig. 6. Image of a FIB cut inside the Al wire interface. A clear granular structure is observed inside the metallization as well as the wire. The void observed just above a transistor channel is believed to be created by the prying of the Al wire.

ture is observed near the bond interface, which has been partly illustrated with the black line. This is naturally a result of the grain refinement during the bonding process.

In Figs. 9 and 10 cross-sectional images of an interface of a failed module is presented.

In Fig. 9 the interface was observed to be in the initial state of a wire bond lift-off. This is indicated by the delamination of the wire from the metallization, and also the initiation of cracks into the

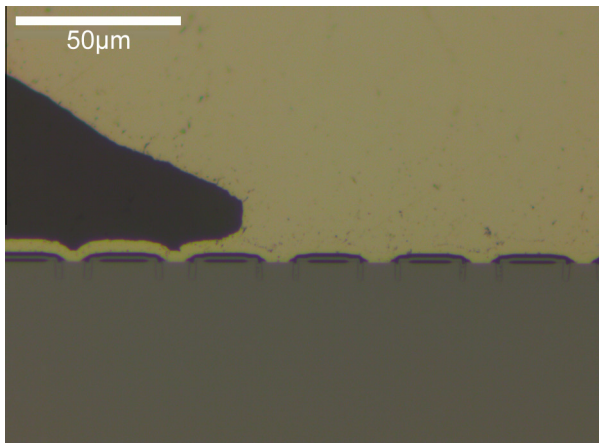


Fig. 7. Ordinary BF microscopy image of the interface between Al wire type B and the IGBT chip after micro-sectioning but prior to etching.

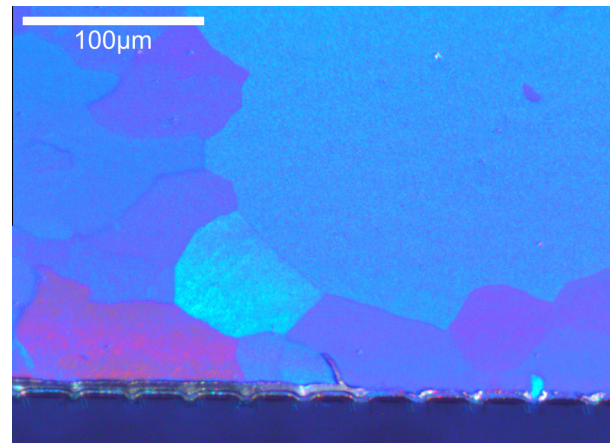


Fig. 10. Cross-sectional image of the sample from Fig. 9 subjected to electro-etching to see the granular structure.

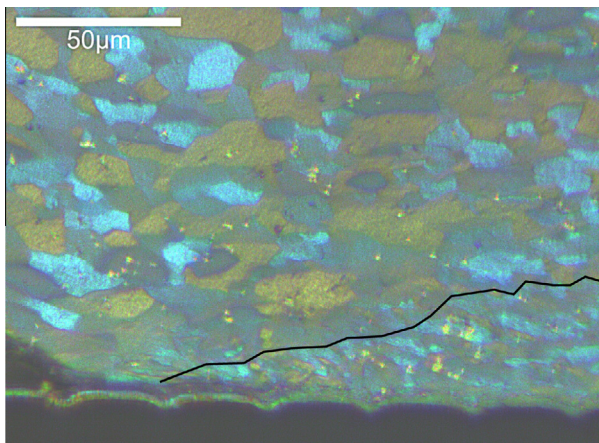


Fig. 8. Microscopy image, of the interface between IGBT and Al wire after etching, obtained using polarized light. The solid line is drawn to visualize the interface formed during the bonding.

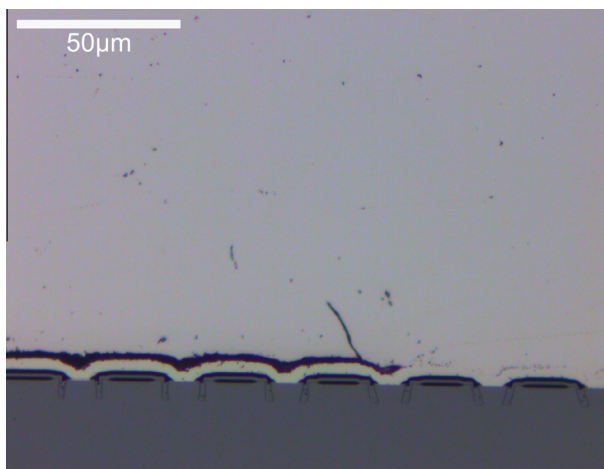


Fig. 9. Cross-sectional image of the heel of a wire bond in a failed module.

wire. The delamination becomes apparent by comparing Figs. 7 and 10.

In Fig. 10 the same interface is presented after being exposed to electro-etching. This has promoted the granular structure of the

interface, and as discussed in Section 2.1 the fracture is clearly seen to propagate at the grain boundaries.

5. Discussion

The results obtained using ordinary SEM combined with FIB yielded a description of the component composition as well as a high resolution characterization of the grain structure. The size of the wire, however, limits the possibilities. Either the wire needs to be removed before or the characterization is limited to the interface edge. The wire removal was observed to damage the interface, and thereby rendering results unusable. The study of the interface edge is simply not sufficient for a detailed description of the interface quality or state.

Instead, the micro-sectioning approach combined with optical microscopy is proposed for characterization of geometries on this scale. The electro-etched images combined with polarized light provide high contrast showing the granular structure of the interface. This enables the possibility of identifying the grain refinement region and thereby the interface quality. Furthermore, the method was shown to be able to identify failure mechanisms and the present state of the given failure. The identification of the bond quality should be directly usable parallel to module fabrication, and the latter could be employed to establish reliable lifetime estimations. However, the lack of resolution limits the grain structure analysis to the wire itself and an identification of the grain refinement area. Meaning that the investigation of the metallization and similar elements on the same scale must be carried out with more advanced techniques like EBSD.

A final remark on the micro-sectioning approach presented in this paper is of course that all steps are severely damaging to the component in question. And, therefore, the method is not suitable for making many sample investigations during production. But the method shows good applicability to examine selected samples for quality investigation as well as damaged modules for failure identification.

6. Conclusion

A micro-sectioning approach for optical or electron microscopy characterization of interfaces in electronic components is developed and described. This technique includes mechanical cutting, removal of unnecessary parts, mechanical and chemical polishing, and finally electro-etching.

The developed approach gives a possibility to obtain resolution on the μm scale and, in particular, to investigate metal grain structure and possible imperfections in the Al wires, and the interface. The method is shown to be able to identify interface related failure mechanisms as well as the present quality of the interface. However, to go to higher resolution (below $1\ \mu\text{m}$), e.g. inside the chip metallization more advanced techniques like EBSD are needed.

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References

- [1] Kanert W. *Microelectron Reliab* 2012;52:2336–41.
- [2] Schilling O, Schfer M, Mainka K, Thoben M, Sauerland F. *Microelectron Reliab* 2012;52:2347–52.
- [3] Czerny B, Lederer M, Nagl B, Trnka A, Khatibi G, Thoben M. *Microelectron Reliab* 2012;52:2353–7.
- [4] Goehre J, Schneider-Ramelow M, Geissler U, Lang K. In: CIPS, 3.4.
- [5] Geiler U, Schneider-Ramelow M, Reichl H. *IEEE Trans Compon Packag Technol* 2009;32:794–9.
- [6] Guth K, Siepe D, Görlich J, Torwesten H, Roth R, Hille F, Umbach F. In: PCIM Europe. p. 232–7.
- [7] Hansen N. *Scr Mater* 2004;51:801–6.
- [8] Voort GV. *ASM handbook. ASM international of etallography and microstructures*, vol. 9; 2004.
- [9] Perryman E, Lack J. *Nature* 1951;167:479.
- [10] Lutz J, Scheuermann U, Schlangenotto H, Doncker R. *Semiconductor power devices – physics, characteristics, reliability*. Springer-Verlag; 2011.